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*Wang, Z.; Guggenbuhl, W.;*  
Electronics Letters , Volume: 25 , Issue: 10 , 11 May 1989  
Pages:673 - 675

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#### 2 A CMOS current-mirror amplifier with compact slew rate enhancement circuit for large capacitive load applications

*Hoi Lee; Mok, P.K.T.;*  
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium , Volume: 1 , 6-9 May 2001  
Pages:220 - 223 vol. 1

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#### 3 Fully balanced CMOS current-mode circuits

*Zele, R.H.; Allstot, D.J.; Fiez, T.S.;*  
Solid-State Circuits, IEEE Journal of , Volume: 28 , Issue: 5 , May 1993  
Pages:569 - 575

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#### 4 A 17-ns 4-Mb CMOS DRAM

*Nagai, T.; Numata, K.; Ogihara, M.; Shimizu, M.; Imai, K.; Hara, T.; Yoshida, Saito, Y.; Asao, Y.; Sawada, S.; Fujii, S.;*  
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 11 , Nov. 1991  
Pages:1538 - 1543

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**5 A block-oriented RAM with half-sized DRAM cell and quasi-folded da  
line architecture**

*Kimura, K.; Sakata, T.; Itoh, K.; Kaga, T.; Nishida, T.; Kawamoto, Y.;*  
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 11 , Nov. 1991  
Pages:1511 - 1518

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**6 Single-point-detection slew-rate enhancement circuits for single-sta  
mplifiers**

*Hoi Lee; Mok, P.K.T.;*  
Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium  
on , Volume: 2 , 26-29 May 2002  
Pages:II-831 - II-834 vol.2

[Abstract] [PDF Full-Text (569 KB)] **IEEE CNF**

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**7 An experimental 1.5-V 64-Mb DRAM**

*Nakagome, Y.; Tanaka, H.; Takeuchi, K.; Kume, E.; Watanabe, Y.; Kaga, T.;  
Kawamoto, Y.; Murai, F.; Izawa, R.; Hisamoto, D.; Kisu, T.; Nishida, T.; Takei,  
E.; Itoh, K.;*  
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 4 , April 1991  
Pages:465 - 472

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